IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Wai Lo
David Chan

Serial No. :	10/702,165	**Group Art Unit :**	2824
Filed :	November 04, 2003	**Examiner :**	Smith, Bradley
For :	Thin Film CMOS Calibration Standard Having Protective Cover Layer	**Atty Docket :**	LSI1P191D1 / 02-0186/1D

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Mark Salvatore

September 30, 2004 — Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Timothy Croll

Reg. No. 36,771

Date: 28 Sept 04